	Application No.	Applicant(s)
Notice of Allowability	09/760,063	HARER ET AL.
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/20/2005*.

2. ☒ The allowed claim(s) is/are *1-36*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some*   c) ☐ None   of the:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

        3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

    * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

        1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____ .

    (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of

        Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)

2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)

3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____

4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application (PTO-152)

6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .

7. ☒ Examiner's Amendment/Comment

8. ☒ Examiner's Statement of Reasons for Allowance

9. ☐ Other _____ .

DETAILED ACTION

1.   Claims 1-36 were examined.

Allowable Subject Matter

2.   Claims 1-36 are allowed.

Examiner's Amendment

3   An examiner's amendment to the record appears below. Should the changes

and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be

submitted no later than the payment of the issue fee.

The change is as follows:

Specification, pg.17, line 14, after "goal states" insert element -- 130 -- .

3.   The following is an examiner's statement of reasons for allowance:

While US Patent 4,698,587 (claims 1 and 9) teaches a method of verifying a design for

a microcircuit; US Patent 6,102,959 (claims 1,9 and 17) teaches beginning [a] random

simulation of a sequence of states of a microcircuit design by inputting a sequence of

random input vectors to a random simulation model to obtain a sequence of random

simulation states; US Patent 5,983,182 (claim 9) teaches a data processing; US Patent

6,829,753 (claim 25) teaches a computer program product comprising a computer

usable medium having a computer readable code embodied therein for verifying a

design for a microcircuit, the computer program product, none of these references,

taken either alone or in combination, with the prior art of record disclosing a

(claim 1) "monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation of a sequence of states of said microcircuit design; beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation states in a formal simulation model of said microcircuit design; monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design; resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit desired caused by inputting said random input vector sequence to said random simulation model; testing for whether a goal state has been reached; and recording an indication that a goal state has been reached; and recording an indication that a goal sate has been reached, that can be used by a user, if a goal state has been found,"

(claim 9) " monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation of a sequence of states of said microcircuit design; beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation states in a formal simulation model of said microcircuit design; monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random

simulation of states of said microcircuit design; resuming said generation of said

random input vector sequence for said random simulation model of a microcircuit design

and said simulating of a sequence of random simulation states of said microcircuit

design caused by inputting said random input vector sequence to said random

simulation model; testing for whether a goal state has been reached; and recording an

indication that a goal sate has been reached, that can be used by a user, if a goal state

has been found,"

(claim 17) "random input vectors to a random simulation model to obtain a sequence of

random simulation states; a circuit configured for monitoring a simulation coverage

progress metric to determine on a basis of said sequence of random simulation states a

preference for beginning formal simulation of a sequence of states of said microcircuit

design; a circuit configured for beginning formal simulation of a sequence of states of

said microcircuit design by using formal simulation methods to simulate a sequence of

formal simulation states in a formal simulation model of said microcircuit design; a

circuit configured for monitoring a formal coverage progress metric to determine on a

basis of said sequence of formal simulation states a preference for resuming random

simulation of states of said microcircuit design; and a circuit configured for resuming

said generation of said random input vector sequence for said random simulation mode

of a microcircuit design and said simulating of a sequence of random simulation states

of said microcircuit design caused by inputting said random input vector sequence to

said random simulation model; a circuit configured for testing for whether a goal state

has been reached; and a circuit configured for recording an indication that a goal state

has been reached, that can be used by a user, if a goal state has been found,"

(claim 25) "computer readable program code devices configured to cause a computer to

effect random simulation of a sequence of states of a microcircuit design by inputting a

sequence of random input vectors to a random simulation model to obtain a sequence

of random simulation states; computer readable program code devices configured to

cause a computer to effect monitoring of a simulation coverage progress metric to

determine on a basis of said sequence of random simulation states a preference for

beginning formal simulation of a sequence of states of said microcircuit design;

computer readable program code devices configured to cause a computer to effect

beginning formal simulation of a sequence of states of said microcircuit design by using

formal simulation methods to simulate a sequence of formal simulation states in a

formal simulation model of said microcircuit design; computer readable program code

devices configured to cause a computer to effect monitoring a formal coverage progress

metric to determine on a basis of said sequence of formal simulation states a

preference for resuming random simulation of states of said microcircuit design;

computer readable program code devices configured to cause a computer to effect

resuming said generation of said random input vector sequence for said random

simulation model of a microcircuit design and said simulating of a sequence of random

simulation states of said microcircuit design caused by inputting said random input

·vector to said random simulation model; computer readable program code devices

configured to cause a computer to effect testing for whether a goal state has been

reached; and computer readable program code devices configured to cause a computer

to effect recording an indication that a goal state has been reached, the can be used by

a user, if a goal state has been found,"

in combination with the remaining elements and features of the claimed invention. It is

for these reasons that the applicants' invention defines over the prior art of record.

Any comments considered necessary by applicant must be submitted no later

than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on

Statement of Reasons for Allowance".

Correspondence Information

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-

3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact

examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to

questions regarding access to the Private PAIR system, contact the Electronic Business

Center (EBC) (toll-free (866-217-9197)).

March 2, 2006

TS

Paul L. Rodriguez   3/3/06
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Primary Examiner
Art Unit 2125